Patent Claims

1. An IR (incremental redundancy) memory for an EGPRS (enhanced general packet radio service) receiver of a mobile station (MS), which receives data from a base station (BS) via a data transmission channel,
the IR memory (1) having:
a) a first memory area (1a) for buffer-storing a specific number of data blocks with a predetermined first data resolution (R_1);
b) a second memory area (1b) for buffer-storing erroneously decoded data blocks,
characterized
in that
c) the second memory area (1b) stores the erroneously decoded data blocks with a second data resolution (R_2), which is lower than the first data resolution (R_1).

2. The IR memory as claimed in claim 1,
characterized
in that the number of data blocks that can be stored in the first memory area (1a) of the IR memory (1) depends on the internal signal delay within the mobile station (MS).

3. The IR memory as claimed in claim 1,
characterized
in that the number of data blocks that can be stored in the second memory area (1b) of the IR memory (1) depends on the polling period of the data transmission channel and on the round trip delay.

4. The IR memory as claimed in claim 1,
characterized
in that the second data resolution (R_2) can be set

adaptively.

5. The IR memory as claimed in claim 4, characterized in that the second data resolution (R_2) with which the erroneously decoded data blocks are stored in the second memory area (1b) of the IR memory (1) can be set in a manner dependent on a burst data transmission signal quality measured by the receiver.

6. The IR memory as claimed in claim 4, characterized in that the second data resolution (R_2) can be changed over between the different resolution levels.

7. The IR memory as claimed in claim 6, characterized in that the resolution levels of the second data resolution are 2 bits, 3 bits or 4 bits.

8. The IR memory as claimed in claim 1, characterized in that the first data resolution (R_1) is 5 bits.

9. The IR memory as claimed in one of the preceding claims, characterized in that the IR memory (1) is connected, on the input side, to a reception buffer memory for data blocks.

10. The IR memory as claimed in one of the preceding claims, characterized in that the IR memory is connected to a decoder on the output side.

11. The IR memory as claimed in one of the preceding claims,
characterized
in that the data blocks are RLC (radio link control) data blocks.

12. The IR memory as claimed in one of the preceding claims,
characterized
in that the data blocks are MCS-coded.